AMENDMENTS TO THE CLAIMS

1. (Previously Presented) A method for clearing the memory of a Field Programmable Gate Array ("FPGA") Integrated Chip ("IC"), comprised of a plurality of cores, said method comprising:

clearing memory of said plurality of cores;

sequentially verifying completion of said clearing memory act for each core of said plurality of cores;

providing a programming ready signal to all cores of said plurality of cores when a last core of said plurality of cores has completed said clearing memory act;

providing an enable memory clear query signal to a first core of said plurality of cores;

clearing memory of said plurality of cores;

determining whether said first core has completed its said clearing memory act;

providing a first core memory cleared signal, if said first core has completed its said clearing memory act;

providing a first core memory cleared out signal;

repeating in a sequential manner the acts of determining whether a next core of said plurality of cores has completed its said clearing memory act, providing a said next core memory cleared signal , if said next core has completed its clearing memory act, and providing a said next core memory cleared out signal, until said last core has completed its clearing memory act;

providing a said last core's memory cleared signal; and

providing a said programming read signal to said all cores.

2. (Cancelled)

3. (Original) A method for sequentially programming with bitstream data each core of a plurality of cores in an FPGA IC, said method comprising:

sending said bitstream data to a first core of said plurality of cores;

sending the balance of said bitstream data to a next core of said plurality of cores after said first core has received its portion of bitstream data;

repeating in a sequential manner the acts of sending a balance of said bitstream data to a following core of said plurality of cores after an immediately preceding core of said plurality of cores has received its portion of bitstream data, until a last core of said plurality of cores has received its portion of bitstream data; and

sending a program start signal to all cores of said plurality of cores.

4. (Original) The method of Claim 3 further comprising:

providing to said first core an enable programming complete query signal;

sending said bitstream data to said first core;

providing a first core programmed signal, when said first core has received all its said bitstream data;

providing a program ok out signal;

sending the balance of said bitstream data from said first core to a next core of said plurality of cores;

repeating the acts of providing a next core programmed signal, when said next core has received all its said bitstream data, providing a next core program ok out

signal, sending the balance of said bitstream data from a said next core to a subsequent core of said plurality of cores, in a sequential manner until a last core of said plurality of cores has received its bitstream data;

providing a said last core programmed signal; and

providing a run program signal to said all cores.

5. (Original) An FPGA IC comprising:

a plurality of cores, wherein each core comprises:

an enable memory clear query signal coupled to an input of a first logic module;

a power up module coupled to an input of said first logic module;

a memory cleared out signal coupled to an output of said first logical module;

a programming module coupled to a programming ready signal;

wherein the memory cleared out signal of each non-last core is coupled to the enable memory clear query signal of a subsequent core; and

wherein the memory cleared out signal of a last core is coupled to said programming ready signal of each core.

6. (Original) The plurality of cores of Claim 5, wherein each core further comprises:

a program okay out signal coupled to a second logic module;

a core programmed signal coupled to said programming module and to an input of said second logic module;

a program okay out signal coupled to the output of said second logic module;

a data out signal coupled to said programming module

a data in signal coupled to each non-first core said programming module;

a start up module coupled to a run program signal; and

wherein each non-last core said program okay out signal is coupled to a subsequent core's enable programming complete query signal, wherein each non-first core data in signal is coupled to said data out signal of a preceding core; wherein a first core's programming module is coupled to a data bus interface, and wherein said program okay out signal of a last core is coupled to said run program signal of each core.

7. (Original) The IC of claim 6, wherein a data fetch clock signal couples each adjacent core's programming module.

8. (Original) The IC of claim 6 wherein the first and second logic units are AND gates.

9. (Original) The IC of claim 6, wherein the data bus interface is a serial interface.

10. (Original) The IC of claim 6, wherein the data bus interface is a parallel interface.

11. (Original) An FPGA IC comprised of a plurality of cores, said IC comprising:

means for providing an enable memory clear query signal to a first core of said plurality of cores;

means for clearing memory of said plurality of cores;

means for determining whether said first core has completed its said clearing memory act;

means for providing a first core memory cleared signal, if said first core has completed its said clearing memory act;

means for providing a first core memory cleared out signal;

means for repeating in a sequential manner the acts of determining whether a next core of said plurality of cores has completed its said clearing memory act, providing a said next core memory cleared signal , if said next core has completed its clearing memory act, and providing a said next core memory cleared out signal, until said last core has completed its clearing memory act;

means for providing a said last core's memory cleared signal; and

means for providing a said programming read signal to said all cores.

12. (Original) An FPGA IC with a plurality of cores, said IC comprising:

means for providing to said first core an enable programming complete query signal;

means for sending said bitstream data to said first core;

means for providing a first core programmed signal, when said first core has received all its said bitstream data;

means for providing a program ok out signal;

means for sending the balance of said bitstream data from said first core to a next core of said plurality of cores;

means for repeating the acts of providing a next core programmed signal, when said next core has received all its said bitstream data, providing a next core program ok out signal, sending the balance of said bitstream data from a said next core to a subsequent core of said plurality of cores, in a sequential manner until a last core of said plurality of cores has received its bitstream data;

means for providing a said last core programmed signal; and

means for providing a run program signal to said all cores.

13. (Cancelled)

14. (Previously Presented) A method for clearing the memory of an FPGA IC, comprised of one core, said method comprising:

clearing memory of said core;

verifying completion of said clearing memory act of said core;

providing a programming ready signal to said core when said core has completed said clearing memory act;

providing an enable memory clear query signal to said core;

clearing memory of said core;

determining whether said core has completed its said clearing memory act;

providing a core memory cleared signal, if said core has completed its said clearing memory act;

providing a core memory cleared out signal; and

providing a said programming read signal to said core.

15. (Cancelled)

16. (Currently Amended) A method for programming with bitstream data a core in a FPGA IC, said method comprising:

sending said bitstream data to said core; ~~and~~

sending a program start signal to said core;

providing to said core an enable programming complete query signal;

sending said bitstream data to said core;

providing a core programmed signal, when said core has received all its said bitstream data;

providing a program ok out signal;

providing a core programmed signal; and

providing a run program signal to said core.

17. (Cancelled)

18. (Original) An FPGA IC comprising:

a core, wherein said core comprises:

an enable memory clear query signal coupled to an input of a first logic module;

a power up module coupled to an input of said first logic module;

a memory cleared out signal coupled to an output of said first logical module;

a programming module coupled to a programming ready signal; and

wherein the memory cleared out signal of said core is coupled to said programming ready signal of said core.

19. (Original) The core of Claim 18, wherein said core further comprises:

a program okay out signal coupled to a second logic module;

a core programmed signal coupled to said programming module and to an input of said second logic module;

a program okay out signal coupled to the output of said second logic module;

a start up module coupled to a run program signal; and

wherein said core's programming module is coupled to a data bus interface, and wherein said program okay out signal of said core is coupled to said run program signal of said core.

20. (Original) The IC of claim 19 wherein the first and second logic units are AND gates.

21. (Original) The IC of claim 19, wherein the data bus interface is a serial interface.

22. (Original) The IC of claim 19, wherein the data bus interface is a parallel interface.

23. (Original) An FPGA IC comprised of a core, said IC comprising:

means for providing an enable memory clear query signal to said core;

means for clearing memory of said core;

means for determining whether said core has completed its said clearing memory act;

means for providing a core memory cleared signal, if said core has completed its said clearing memory act;

means for providing a said core memory cleared out signal;

means for providing a said core memory cleared signal; and

means for providing a said core programming read signal.

24. (Original) An FPGA IC with a core, said IC comprising:

means for providing to said core an enable programming complete query signal;

means for sending said bitstream data to said core;

means for providing said core programmed signal, when said core has received all its said bitstream data;

means for providing a program ok out signal; and

means for providing a run program signal to said core.

25. (Cancelled)